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It is an object of the invention to provide a device for testing logic integrated circuits which requires only little additional surface area on the IC to be tested (DUT), that is, without degrading the test performance and without using large test memories.

The object of the invention is achieved in that an arrangement for the testing of integrated circuits is provided with a test system which includes a test vector generator for generating test vectors and a logic component provided on the IC to be tested.

In the test system there is implemented a test vector generator which is
5 programmable and, therefore, is capable of generating test vectors which are transferred to the DUT. A programmable algorithm is implemented in the test vector generator. The test vectors traverse a logic component to be tested and are transferred to a test response analysis unit. The test response vectors traverse a sequential logic circuit in said test response analysis unit, are compressed and a check sum is formed. The check sum is transferred, by way of a
10 test control block, to the test system in which the check sum is compared with a reference check sum.

The test vectors are generated in real time as in the BIST system, be it now in the test system. The large and expensive memory for the test vectors in the test system is replaced by the programmable algorithmic test vector generator which generates the test
15 vectors. Such a test vector generator includes a processor, notably an arithmetic and logic unit (ALU), and its programming enables the required test vectors to be generated in real time.

This embodiment offers the advantage that testing can be performed at a high speed, because the test system enables fast driving of the DUT and because the amounts of
20 data transferred from the DUT to the test system are small.

The test control block is responsible for the switching over between the various modes. For a test it is necessary to switch over the DUT from the normal mode to the test mode. The test control block controls the switching over of the circuit from a normal mode of operation to a test mode. The test control block then isolates the logic component
25 from a periphery that is not required for a test and controls all control signals and data signals necessary for the transfer of the test vectors from the test system to the DUT and for the transfer of test responses and/or check sums from the DUT to the test system.

The test response analysis unit in a further embodiment of the invention is integrated in the test system together with the programmable algorithmic test vector
30 generator. The programmable algorithmic test vector generator generates, via the processor, test vectors which are transferred to the DUT. The DUT transfers the test response vectors to the test response analysis unit which is included in the test system. The relevant test responses are compressed therein so as to form a check sum which is compared with a reference check sum in the test system.

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This implementation has the drawback that integration of the test response analysis unit in the test system leads to a loss of speed. The DUT has to transfer all test response vectors to the test system and requires a corresponding amount of time for this purpose. However, an advantage is achieved in that logic circuits already in existence can be
5 tested by means of such a test system without it being necessary to redesign such circuits.

When the test response analysis unit is implemented in the DUT, ultimately only the check sum will be transferred to the test system by way of the test control block. This has the drawback that fault localization is not possible, because it cannot be deduced why the check sum has been created in its present form. However, if the test response
10 analysis unit is integrated in the test system, the test response vectors are applied directly to the test system after the test vectors have traversed the logic components in the DUT, thus enabling fault localization.

It is a further advantage of the invention that the programming of the test vector generator and its processor readily enables modification of the test vectors. This is not
15 possible in known BIST test arrangements.

The most pronounced advantage of the invention is that the programmable test vector generator is capable of modifying simple test systems so that logic components can be tested by generating pseudo-random test vectors as well as deterministic test vectors.

In the embodiment of the invention as disclosed in claim 2 it is necessary to
20 design the test response analysis unit so as to be included in the DUT.

For the embodiment of the invention as disclosed in claim 4 it is not necessary to design the DUT for the test, because the test response analysis unit is integrated in the test system.

External circumstances determine which of the above alternatives is used for
25 the testing of logic components. In this respect it is to be taken into account how much time is available for the test, whether an additional design is possible for the test response analysis unit, etc.

An embodiment will be described in detail hereinafter with reference to the drawing. Therein:

30 Fig. 1 shows a test system with a test vector memory in accordance with the present state of the art,

Fig. 2 shows a BIST test arrangement in accordance with the present state of the art,

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transferred, via the connection 11, to the test response analysis unit 5 in the test system 2 in which the test response vectors are compressed so as to form a check sum. The check sum is compared with a reference checksum, stored in the test system, in order to produce a test result.

- 5 The processor 12 provides the generating of the test vectors in real time as well as the compression of the test response vectors transferred by the DUT 1.

- A Multiple Input Shift Register (MISR) constitutes a hardware implementation of a test response analysis unit. It compresses all outputs into a signature or check sum. This method is also referred to as a Cyclic Redundancy Check (CRC). A further implementation
10 of a test response analysis unit is formed by an adder which forms each time a check sum. The test response analysis unit can also be realized by means of a processor.

- There are several possibilities for generating the result of such a test or the fault indication. The reference check sum, calculated in advance, may be stored in the DUT 1, in which case it is also compared in this DUT 1, and a pass or reject decision is output as a
15 fault decision. It is also possible to store this reference check sum in the test system wherein the comparison is then also performed.

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